REMARKS

Claims 1 through 16, 19 through 24, 26 through 41 and 44 through 49 are currently pending in the application.

This amendment is in response to the Office Action of March 25, 2005.

Information Disclosure Statement(s)

Applicants note the filing of an Information Disclosure Statement herein on August 29, 2001 and note that a copy of the PTO-1449 was not returned with the outstanding Office Action. Applicants respectfully request that the information cited on the PTO-1449 (which is the same as that of record to that date in the parent application hereto) be made of record herein.

Supplemental Information Disclosure Statement

Please note that Supplemental Information Disclosure Statements were filed herein on August 22, 2002 and September 9, 2004, and that no copy of the PTO-1449s were returned with the outstanding Office Action. Applicants respectfully request that the information cited on the PTO-1449s be made of record herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Yamada et al. (U.S. Patent 5,864,178) in view of Hoge et al. (U.S. Patent 4,388,132)

Claims 1 through 16, 19 through 24, 26 through 41 and 44 through 49 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamada et al. (U.S. Patent 5,864,178) in view of Hoge et al. (U.S. Patent 4,388,132). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants assert that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of

the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Turning to the cited prior art Yamada et al. reference, teaches or suggests a semiconductor device comprising a wiring circuit board and a semiconductor chip mounted through a bump electrode on the circuit board, a space between the circuit board and the semiconductor chip as well as a periphery of the semiconductor chip being encapsulated with a resin containing filler. In FIGS. 56A through 56D a semiconductor chip 201 is mounted on a wiring circuit board 202 using bumps 203 with the semiconductor chip 201 having a layer of a first resin 204 constituting a laminate of encapsulation resin, a second layer of resin 205 on the wiring circuit board 202 constituting a laminate of encapsulation resin, a third encapsulation resin 206 constituting a laminate of encapsulation resin applied to a portion of the second layer of resin 205, a polymer film 207 formed on the semiconductor chip 201, and a polymer film 208 formed on the wiring circuit board 202. Nowhere does Yamada et al. describe the semiconductor chip 201 having at least a portion of said active surface having a wetting agent layer of about a monolayer thick thereon, said wetting agent layer wetable by a polymeric material. At best, Yamade et al. describe that solely the first layer of encapsulation resin 204, second layer of encapsulation resin 205, and third encapsulation resin 206 may include a silane coupling agent therein mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board as a wetting agent layer. Nowhere in the Yamada et al. reference is there any description whatsoever directed to any of the encapsulation resins 204, 205, and 206 acting as a wetting agent under any circumstances.

The Hoge et al. reference teaches or suggests the use of a coupling agent 60 applied to a film 20 prior to the film 20 contacting an adhesive 40 applied to a region 11 of a chip 10. Nowhere in the Hoge et al. reference is there any teaching or suggestion to apply the coupling agent 60 to the region 11 of the chip 10.

Applicant asserts that any combination of the Yamada et al. reference and the Hoge et al. reference establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the

claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 because any combination of such cited prior art, at the least, fails to teach or suggest all of the claim limitations of the claimed inventions and because the suggestion to make the claimed combination and the reasonable expectation of success are not found in the cited prior art but, are solely based on Applicant's disclosure.

For instance, Applicant asserts that the any combination of the Yamada et al. reference and the Hoge et al. reference does not teach or suggest the claim limitations of the claimed inventions set forth in independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 calling for "the semiconductor device having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer thickness thereon comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor device, said wetting agent layer having a thickness of about a monolayer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent located on a portion of said active surface of said semiconductor device comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on at least a portion of said active surface of said semiconductor device comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material, the underfill material essentially filling a volume between said wetting agent layer and said upper surface of said substrate", "a wetting agent layer provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor device and on said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow

process and a curing process for a material", "the semiconductor die having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer in thickness thereon, said wetting agent layer wetable by a polymeric material, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor die, said wetting agent layer having a thickness of about a monolayer and wetable by a polymeric material, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", and "a wetting agent layer provided on said active surface of said semiconductor die and on said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material".

In contrast to the claimed inventions, Applicant asserts that nowhere does the combination of the Yamada et al. reference and the Hoge et al. reference describe a wetting agent used on a portion of a semiconductor device, semiconductor die, or substrate in any manner. At best, the Yamada et al. reference discusses the use of silane coupling agent mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board. At best, the Hoge et al. reference teaches or suggests the use of a coupling agent applied to an adhesive. The claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are not directed to the use of a silane coupling agent in the formulation of an encapsulation resin or a coupling agent applied to the surface of an encapsulation resin containing a silane coupling agent in the formulation thereof. Therefore, any combination of the Yamada et al. reference and the Hoge et al. reference

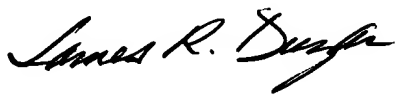
cannot and does establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48. Accordingly, independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are allowable as well as the dependent claims therefrom.

Further, Applicant asserts that any combination of the Yamada et al. reference and the Hoge et al reference is a hindsight reconstruction of the Applicant's claimed inventions by picking and choosing among the cited prior art based solely upon Applicant's disclosure because the cited prior art fails to suggest any reason for any combination thereof and, even if combined, does not teach or suggest the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48. Such hindsight is evidenced by the attempted modification of the Yamada et al. reference to include the use of a coupling agent applied to an adhesive layer. The Yamada et al. reference contains no adhesive layer. Therefore, any combination of the Yamada et al. reference and the Hoge et al. reference cannot and does establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48. Accordingly, independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are allowable as well as the dependent claims therefrom.

Applicants submit that claims 1 through 16, 19 through 24, 26 through 41 and 44 through 49 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 1 through 16, 19 through 24, 26 through 41 and 44 through 49 and the case passed for issue.

Respectfully submitted,



James R. Duzan
Registration No. 28,393
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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